With CMOS technology scaling down, static random access memories (SRAMs) consume more than 90 % of chip area and power consumption in modern microprocessor designs and system-on-chip applications. In order to achieve lower power consumption and less area for SRAMs, 4T SRAM structure can be used. However, the conventional silicon 4T SRAM suffers low static noise margin (SNM) and other stability issues compared with commonly used 6T SRAM. In order to improve the SNM and the robustness of 4T SRAM, in this paper we propose a novel hybrid silicon/carbon nanotube (CNT) 4T SRAM structure. The latch transistors in silicon 4T SRAM structure are replaced with carbon nanotube field effect transistors (CNFETs). The proposed design reduces 58 % cell area compared with silicon 6T SRAM and features improved performance and stability compared with silicon 4T SRAM. With the benefits of low OFF current and high ON current from CNFET devices, the proposed hybrid 4T SRAM has 8.3x faster reading speed, 2.5x faster writing speed, 34.5 % reduction for reading power and 24 % reduction for writing power compared with silicon 4T SRAM. The SNM of the proposed design is increased to 6x and 1.11x compared with silicon 4T and 6T SRAM respectively.

Your computer probably uses both static RAM and dynamic RAM at the same time, but it uses them for different reasons because of the cost difference between the two types. If you understand how dynamic RAM and static RAM chips work inside, it is easy to see why the cost difference is there,­ and you can also understand the names.

Dynamic RAM is the most common type of memory in use today. Inside a dynamic RAM chip, each memory cell holds one [bit](http://computer.howstuffworks.com/bytes.htm) of information and is made up of two parts: a [transistor](http://electronics.howstuffworks.com/transistor.htm) and a [capacitor](http://electronics.howstuffworks.com/capacitor.htm). These are, of course, extremely small transistors and capacitors so that millions of them can fit on a single memory chip. The capacitor holds the bit of information -- a 0 or a 1 (see [How Bits and Bytes Work](http://computer.howstuffworks.com/bytes.htm) for information on bits). The transistor acts as a switch that lets the control circuitry on the memory chip read the capacitor or change its state.

A capacitor is like a small bucket that is able to store electrons. To store a 1 in the memory cell, the bucket is filled with electrons. To store a 0, it is emptied. The problem with the capacitor's bucket is that it has a leak. In a matter of a few milliseconds a full bucket becomes empty. Therefore, for dynamic memory to work, either the CPU or the **memory controller** has to come along and recharge all of the capacitors holding a 1 before they discharge. To do this, the memory controller reads the memory and then writes it right back. This refresh operation happens automatically thousands of times per second.

This refresh operation is where dynamic RAM gets its name. Dynamic RAM has to be dynamically refreshed all of the time or it forgets what it is holding. The downside of all of this refreshing is that it takes time and slows down the memory.

Static RAM uses a completely different technology. In static RAM, a form of flip-flop holds each bit of memory (see [How Boolean Gates Work](http://computer.howstuffworks.com/boolean.htm) for detail on flip-flops). A flip-flop for a memory cell takes 4 or 6 transistors along with some wiring, but never has to be refreshed. This makes static RAM significantly faster than dynamic RAM. However, because it has more parts, a static memory cell takes a lot more space on a chip than a dynamic memory cell. Therefore you get less memory per chip, and that makes static RAM a lot more expensive.

So static RAM is fast and expensive, and dynamic RAM is less expensive and slower. Therefore static RAM is used to create the CPU's speed-sensitive [cache](http://computer.howstuffworks.com/cache.htm), while dynamic RAM forms the larger system RAM space.

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